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WO 98/42026 A1

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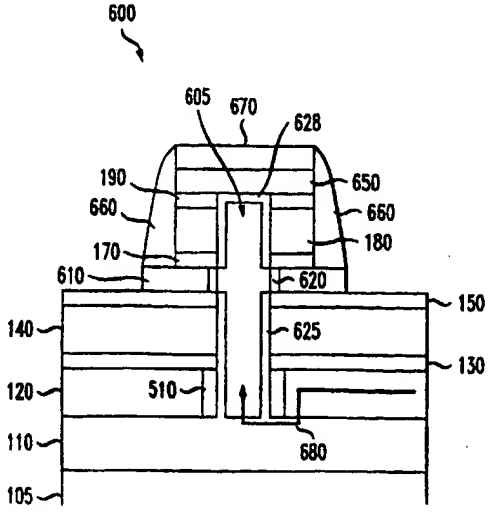
(54) Abstract Title

Vertical replacement gate (VRG) MOSFET with condutive layer adjacent a source/drain region

(57) A vertical replacement gate (VRG) transistor structure comprises first source/drain region (110) on substrate (105), conductive layer (120) adjacent and electrically connected to the first source/drain region (110), second source/drain region (650) located over the first source/drain region (110), and conductive channel (605) extending between two source/drain regions (110, 650). The VRG transistor may have gate (610) located over conductive layer (120), dielectric regions (510) of silicon dioxide located between conductive layer (120) and conductive channel (605), and insulating regions (140,180) located between conductive layer (120) and gate (610), and between gate (610) and second source/drain region (650). The conductive layer (120) may be a metal silicide. The VRG transistor may be used in an integrated circuit structure connected to lateral transistors by interconnects formed in interlevel dielectric layers. The VRG transistor operates by a current (680) moving from conductive layer (120), through first source/drain region (110) and up conductive channel (605) to second source/drain region (650).

FIG. 6



GB 2 366 44

FIG. 2

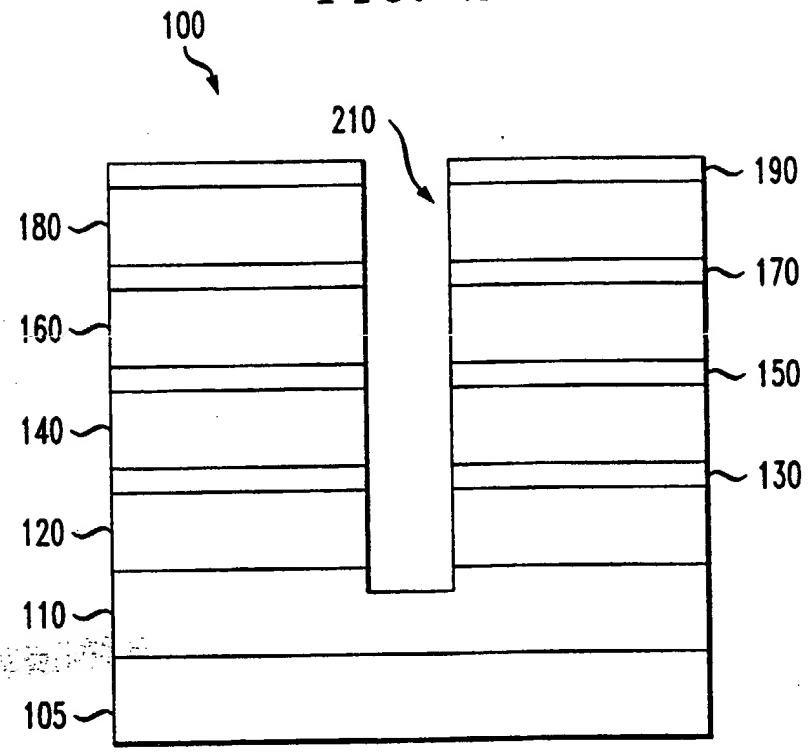

100
210
190
180
170
160
150
140
130
120
110
105

FIG. 3

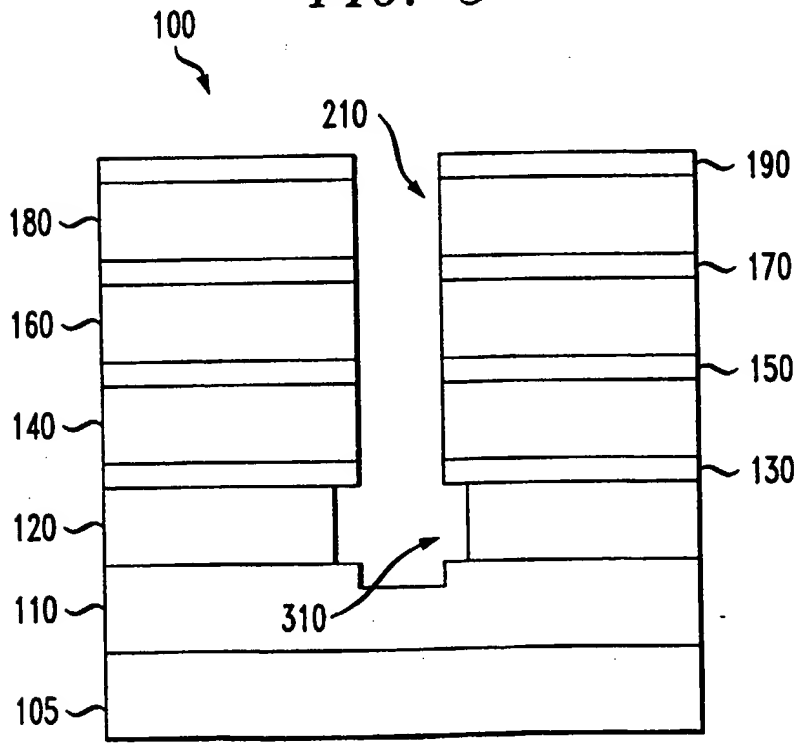
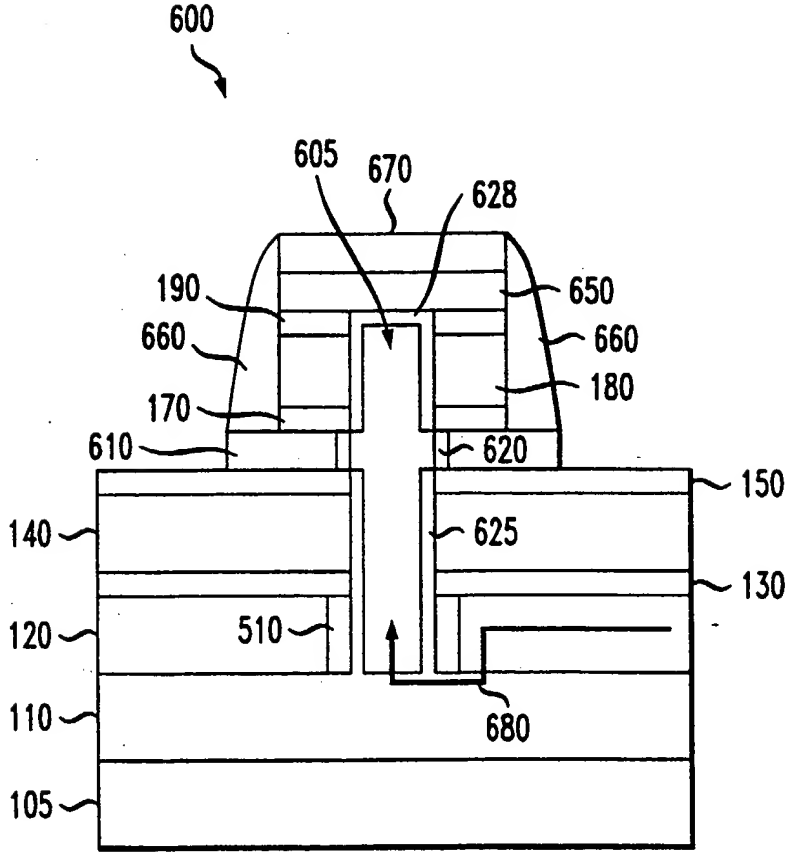

100
210
190
180
170
160
150
140
130
120
310
110
105

FIG. 6


600
605
670
628
190
650
660
660
180
170
610
620
150
140
625
130
120
510
110
680
105

VERTICAL REPLACEMENT GATE (VRG) MOSFET WITH A CONDUCTIVE LAYER ADJACENT A SOURCE/DRAIN REGION AND METHOD OF MANUFACTURE THEREFOR

TECHNICAL FIELD OF THE INVENTION

The present invention is directed, in general, to a semiconductor device and a method of manufacture therefor and, more specifically, to a vertical replacement gate (VRG) metal oxide semiconductor field effect transistor (MOSFET) with a conductive layer adjacent a source/drain region and a method of manufacture therefor.

BACKGROUND OF THE INVENTION

Enhancing semiconductor device performance continues to be a focus of the semiconductor industry. As a result, both smaller device size and increased performance have been identified as desirable manufacturing targets. As device dimensions within semiconductor devices, such as gates within integrated circuits (ICs), continue to shrink, the method for forming such gates has adapted to effectively accomplish the shrinking devices. However, manufacturing limitations have particularly arisen with respect to the lithographic processes currently used to manufacture such shrunken devices. In fact, current lithographic processes have been unable to accurately manufacture devices at the required minimal sizes. Moreover, this is a limitation that the semiconductor industry, to date, has been unable to correct.

In view of the current limitations in the semiconductor manufacturing lithography process, and the desire to manufacture smaller devices, the semiconductor industry

art. The present invention addresses this need.

SUMMARY OF THE INVENTION

To address the above-discussed deficiencies of the prior art, the present invention provides a VRG structure formed on a semiconductor wafer substrate. The VRG structure has a first source/drain region located in a semiconductor wafer substrate, and a conductive layer located adjacent the first source/drain region, a second source/drain region and a conductive channel that extends from the first source/drain region to the second source/drain region. The conductive layer provides an electrical connection to the source/drain region. In a preferred embodiment, the conductive layer has a low sheet resistance that may be less than about 50 Ω/square, and preferably less than about 20 Ω/square, to the first source/drain region. In another embodiment, the VRG structure further comprises a gate located over the conductive layer with the second source/drain region being located adjacent the gate and the conductive layer. In another one embodiment, the conductive channel has a first source/drain region extension and a second source/drain region extension.

Thus, in one aspect, the present invention provides a VRG structure with a conductive layer that is electrically connected to the source/drain region and provides electrical connection to the source/drain region that allows the VRG structure to operate in a more rapid and efficient manner.

The foregoing has outlined, rather broadly, preferred and alternative features of the present invention so that

and filling the trench, including the recesses;

FIGURE 5 illustrates a partial section view of the dielectric regions within the recesses, after removal of the oxide layer;

FIGURE 6 illustrates a partial sectional view of a completed VRG structure in accordance with one embodiment of the present invention; and

FIGURE 7 illustrates a partial sectional view of an integrated circuit, including a conventional transistor and the completed VRG structure illustrated in FIGURE 6.

DETAILED DESCRIPTION

Turning initially to FIGURE 1A, there is illustrated a VRG structure 100 of the present invention, during an initial phase of manufacture. In this particular illustration, a first or bottom source/drain region 110 is conventionally formed in a semiconductor substrate 105. A semiconductor substrate for purposes of the present application may not only include a substrate of the a semiconductor wafer itself, but can also include a substrate of any material deposited on the semiconductor wafer. In the illustrated embodiment, the first source/drain region 110 comprises silicon that has been implanted with a high dose dopant, such as an n-type dopant. However, one having skill in the art knows, obviously, that the first source/drain region 110 may comprise other substances of which may be implanted with different amounts of varying implants.

A conductive layer 120 is conventionally formed adjacent the first source/drain region 110, and more

140 comprises phosphosilicate glass (PSG), but other similar insulating materials may be used. Following the conventional deposition of the second dielectric layer 150, is the deposition of another dielectric layer 160, such as a tetra-ethyl-ortho-silicate (TEOS) layer, a third dielectric layer 170, a second insulating layer 180 and a fourth dielectric layer 190. As discussed earlier, all of the layers 130, 140, 150, 160, 170, 180, 190 may be deposited using conventional PVD and CVD processes, or any other deposition processes known to those who are skilled in the art. In the illustrated embodiment, the dielectric layers 130, 150, 170, 190 are preferably nitride layers. However, other dielectric materials may be used as well. The sequence of the various insulating or dielectric layers discussed above are with respect to a preferred embodiment. It should be understood however, that other embodiments may include different layered or non-layered structures sufficient to form a conductive channel for the VRG as discussed below.

FIGURE 2 illustrates the formation of a trench 210 within the VRG structure 100 illustrated in FIGURE 1B. To accomplish this, the VRG structure 100 is conventionally patterned with photoresist to expose a portion where the trench 210 is desired. The exposed portion of the VRG structure 100 is then subjected to a traditional trench etch which forms the illustrated trench 210. In the illustrated embodiment, the trench 210 is formed down to and partially within the first source/drain region 110. One having skill in the art is familiar with the above-described trenching

conductive channel 605, which preferably comprises doped or undoped silicon. The conductive channel 605 connects the first source/drain region 110 with a second source/drain region 650. The exposed portion of the conductive channel 605 then undergoes a standard VRG-MOSFET process, leaving the completed VRG structure 600 of the present invention, illustrated in FIGURE 6.

The completed VRG structure 600 includes a gate 610 located over, but separated from, the conductive layer 120, the gate 610 having the third dielectric layer 170 deposited thereon. The completed VRG structure 600 also includes a second insulating layer 180 that is deposited over the third dielectric layer 170, a fourth dielectric layer 190 deposited over the second insulating layer 180, the gate 610 and the conductive layer 120, and a second source/drain region 650 deposited over the channel 605, gate 610 and conductive layer 120. The completed VRG structure 600 also has gate dielectrics 620 located between the gate 610 and the conductive channel 605, and conventionally formed first source/drain region extension 625 and second source/drain region extension 628. One having skill in the art knows that the first source/drain region extension 625 and the second source/drain region extension 628 may be formed by solid source diffusion. Dielectric spacers 660 and capping dielectric layer 670, both of which are preferably nitrides, are also conventionally formed to complete the VRG structure 600. FIGURE 6 does not show the gate 610 having a gate contact such that voltages may be applied to the gate 610; however, one having skill in the art knows how to apply

comprise $CoSi_2$ which has a sheet resistance of about 10Ω/square, $TiSi_2$ and TiN. Thus, the low sheet resistance conductive layer 120, regardless of what low sheet resistance conductive metal is used, reduces the first source/drain sheet resistance, which in turn leads to a higher current drive (I_{ON}). This in turn, provides the semiconductor manufacturing industry with the benefit of increased performance without compromising device speed.

Turning briefly to FIGURE 7, with continued reference to FIGURE 6, illustrated is the completed VRG structure 600 located within a conventional integrated circuit 700. The integrated circuit 700 may, in another embodiment, include a conventional lateral transistor 710, such as a complementary metal oxide semiconductor (CMOS) transistor, the transistor 710 having a source 720 and a drain 730. The integrated circuit 700 also includes conventionally formed interconnects 740, 745, 750, 755 formed in interlevel dielectric layers 760 and interconnecting the transistor 710 and VRG structure 600 to form the integrated circuit 700. One having skill in the art knows that multiple VRG structures 600 and transistors 710 could be located within the completed integrated circuit 700. Moreover, as with the conventional transistor 710, the VRG structure 600 is operated by supplying a bias voltage between a combination of the second source/drain region 650, the gate 610 and the conductive layer 120. The voltage may be applied to the conductive layer 120 through the interconnect 740, to the second source/drain region 650 through the interconnect 745 and to the gate through the interconnect 750. During

CLAIMS:

1. A vertical gate transistor, comprising:

a first source/drain region located in a semiconductor wafer substrate; and

a conductive layer located adjacent the source/drain region and providing electrical connection to the source/drain region;

a second source/drain region located over the first source/drain region; and

a conductive channel extending from the first source drain region to the second source/drain region.

2. The vertical gate transistor as recited in Claim 1 further including a gate located over the conductive layer.

3. The vertical gate transistor as recited in Claim 2 further comprising a first insulating region located between the conductive layer and the gate and a second insulating region located between the gate and the second source/drain region.

4. The vertical gate transistor as recited in Claim 3 wherein the first insulating region includes a nitride layer and the second insulating region includes another nitride layer.

5. The vertical gate transistor as recited in Claim 1 further comprising dielectric regions located between the conductive layer and the conductive channel.

6. The vertical gate transistor as recited in Claim 5 wherein the dielectric regions are silicon dioxide regions.

7. The vertical gate transistor as recited in Claim 1 wherein the conductive layer is a metal silicide layer and

a second source/drain region located over the first source/drain region; and

a conductive channel extending from the first source drain region to the second source/drain region; and

interconnect structures formed in interlevel dielectric layers that interconnect the lateral transistors and vertical gate transistors to form an integrated circuit.

16. The integrated circuit as recited in Claim 15 wherein the vertical gate transistors each further include a gate located over the conductive layer.

17. The integrated circuit as recited in Claim 16 further comprising a first insulating region located between the conductive layer and the gate and a second insulating region located between the gate and the second source/drain region.

18. The integrated circuit as recited in Claim 17 wherein the first insulating region includes a nitride layer and the second insulating region includes another nitride layer.

19. The integrated circuit as recited in Claim 16 further comprising dielectric regions located between the conductive layer and the conductive channel.

20. The integrated circuit as recited in Claim 19 wherein the dielectric regions are silicon dioxide regions.

21. The integrated circuit as recited in Claim 15 wherein the conductive layer is a metal silicide layer and is comprised of tungsten silicide.

22. The integrated circuit as recited in Claim 15 wherein the conductive layer is a metal silicide layer and

source/drain region.

30. The method as recited in Claim 29 wherein forming a first insulating region includes forming a nitride layer and forming a second insulating region includes forming another nitride layer.

31. The method as recited in Claim 28 further comprising forming dielectric regions located between the conductive layer and the conductive channel.

32. The method as recited in Claim 31 wherein forming the dielectric regions includes forming dielectric regions comprising silicon dioxide.

33. The method as recited in Claim 27 wherein forming a conductive layer includes forming a metal silicide layer comprising tungsten silicide.

34. The method as recited in Claim 27 wherein forming a conductive layer includes forming a metal silicide layer comprising cobalt silicide.

35. The method as recited in Claim 27 wherein forming a conductive layer includes forming a metal silicide layer comprising titanium silicide.

36. The method as recited in Claim 27 wherein forming a conductive layer includes forming a metal layer.

37. The method as recited in Claim 36 wherein forming a metal layer includes forming a metal layer comprising titanium nitride.

38. The method as recited in Claim 27 wherein forming a conductive layer includes forming a conductive layer having a sheet resistance that is less than about 50 Ω/square.

INVESTOR IN PEOPLE

Application No: GB 0106591.1 **Examiner:** T P Marlow
Claims searched: 1 to 45 **Date of search:** 21 December 2001

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.S): H1K: (KCAV)

Int Cl (Ed.7): H01L

Other: ONLINE: WPI, EPODOC, JAPIO

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
X	WO 98/42026 A1	SIEMENS - see metal silicide conducting layer (110) electrically connected via doped connecting layer (19) to drain (14), and conducting channel (15), source (16) and gate (113') in Fig. 9	1,2,5-13, 15,16, 19-25,27, 28,31-39, 41-45

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
		E	Patent document published on or after, but with priority date earlier